Low Voltage Micropower Quad Operational Amplifier

OP490

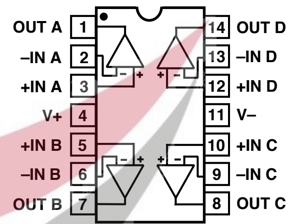
FEATURES

Single/Dual-Supply Operation
- **1.6 V to 36 V**
- **±0.8 V to ±18 V**

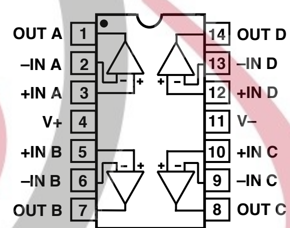
True Single-Supply Operation; Input and Output Voltage Ranges Include Ground
Low Supply Current: 80 µA Max
High Output Drive: 5 mA Min
Low Offset Voltage: 0.5 mA Max
High Open-Loop Gain: 700 V/mV Min
Outstanding PSRR: 5.6 mV/V Min
Industry Standard Quad Pinouts
Available in Die Form

PIN CONNECTION

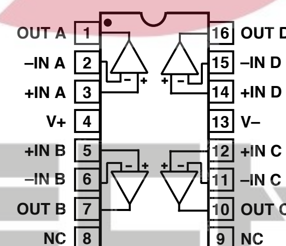
14-Lead Hermetic DIP (Y Suffix)



14-Lead Plastic DIP (P Suffix)



16-Lead SOIC (S Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP490 is a high-performance micropower quad op amp that operates from a single supply of 1.6 V to 36 V or from dual supplies of ±0.8 V to ±18 V. Input voltage range includes the negative rail allowing the OP490 to accommodate input signals down to ground in single-supply operation. The OP490's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

The quad OP490 draws less than 20 µA of quiescent supply current per amplifier, but each amplifier is able to deliver over 5 mA of output current to a load. Input offset voltage is under 0.5 mV with offset drift below 5 µV/°C over the military temperature range. Gain exceeds over 700,000 and CMR is better than 100 dB. A PSRR of under 5.6 µV/V minimizes offset voltage changes experienced in battery-powered systems.

The quad OP490 combines high performance with the space and cost savings of quad amplifiers. The minimal voltage and current requirements of the OP490 make it ideal for battery- and solar-powered applications, such as portable instruments and remote sensors.

REV. C

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OP490–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±1.5 V to ±15 V, T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Conditions	OP490E Min	OP490E Typ	OP490E Max	OP490F Min	OP490F Typ	OP490F Max	OP490G Min	OP490G Typ	OP490G Max	Unit
Input Offset Voltage	V_{OS}			0.2	0.5		0.4	0.75		0.6	1.0	mV
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.4	3.0		0.4	5		0.4	5	nA
Input Bias Current	I_B	V_{CM} = 0 V		4.2	15.0		4.2	20		4.2	25	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15 V, V_O = ±10 V,										
		R_L = 100 kΩ	700	1,200		500	1,000		400	800		V/mV
		R_L = 10 kΩ	350	600		250	500		200	400		V/mV
		R_L = 2 kΩ	125	250		100	200		100	200		V/mV
		V+ = 5 V, V– = 0 V, 1 V < V_O < 4 V										
		R_L = 100 kΩ	200	400		125	300		100	250		V/mV
		R_L = 10 kΩ	100	180		75	140		70	140		V/mV
Input Voltage Range	IVR	V+ = 5 V, V– = 0 V	0/4			0/4			0/4			V
		V_S = ±15 V[1]	–15/+13.5			–15/+13.5			–15/+13.5			V
Output Voltage Swing	V_O	V_S = ±15 V, R_L = 10 kΩ	±13.5	±14.2		±13.5	±14.2		±13.5	±14.2		V
		R_L = 2 kΩ	±10.5	±11.5		±10.5	±11.5		±10.5	±11.5		V
	V_{OH}	V+ = 5 V, V– = 0 V, R_L = 2 kΩ	4.0	4.2		4.0	4.2		4.0	4.2		V
	V_{OL}	V+ = 5 V, V– = 0 V, R_L = 10 kΩ		100	500		100	500		100	500	µV
Common-Mode Rejection Ratio	CMRR	V+ = 5 V, V– = 0 V, 0 V < V_{CM} < 4 V	90	110		80	100		800	100		dB
		V_S = ±15 V, –15 V < V_{CM} < +13.5 V	100	130		90	120		90	120		dB
Power Supply Rejection Ratio	PSRR			1.0	5.6		3.2	10		3.2	10	µV/V
Slew Rate	SR	V_S = ±15 V	5	12		5	12		5	12		V/ms
Supply Current (All Amplifiers)	I_{SY}	V_S = ±1.5 V, No Load		40	60		40	60		40	60	µA
		V_S = ±15 V, No Load		60	80		60	80		60	80	µA
Capacitive Load Stability		A_V = 1		650			650			650		pF
Input Noise Voltage	e_n p-p	f_O = 0.1 Hz to 10 Hz, V_S = ±15 V		3			3			3		µV p-p
Input Resistance Differential Mode	R_{IN}	V_S = ±15 V		30			30			30		MΩ
Input Resistance Common-Mode	R_{INCM}	V_S = ±15 V		20			20			20		GΩ
Gain Bandwidth Product	GBWP	A_V = 1		20			20			20		kHz
Channel Separation	CS	f_O = 10 Hz, V_O = 20 V p-p V_S = ±15 V[2]	120	150		120	150		120	150		dB

NOTES
[1]Guaranteed by CMRR test.
[2]Guaranteed but not 100% tested.
Specifications subject to change without notice

ELECTRICAL CHARACTERISTICS (@ V_S = ±1.5 V to ±15 V, –25°C ≤ T_A ≤ +85°C for OP490E/F, –40°C ≤ T_A ≤ +125°C for OP490G, unless otherwise noted)

Parameter	Symbol	Conditions	OP490E Min	OP490E Typ	OP490E Max	OP490F Min	OP490F Typ	OP490F Max	OP490G Min	OP490G Typ	OP490G Max	Unit
Input Offset Voltage	V_{OS}			0.32	0.8		0.6	1.35		0.8	1.5	mV
Average Input Offset Voltage Drift	TCV_{OS}	V_S = ±15 V		2	5		4			4		µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.8	3		1.0	5		1.3	7	nA
Input Bias Current	I_B	V_{CM} = 0 V		4.4	15		4.4	20		4.4	25	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15 V, V_O = ±10 V,										
		R_L = 100 kΩ	500	800		350	700		300	600		V/mV
		R_L = 10 kΩ	250	400		175	250		150	250		V/mV
		R_L = 2 kΩ	100	200		75	150		75	125		V/mV
		V+ = 5 V, V– = 0 V, 1 V < V_O < 4 V										
		R_L = 100 kΩ	150	280		100	220		80	160		V/mV
		R_L = 10 kΩ	75	140		50	110		40	90		V/mV
Input Voltage Range	IVR	V+ = 5 V, V– = 0 V	0.3/5			0.3/5			0.3/5			V
		V_S = ±15 V*	–15/+13.5			–15/+13.5			–15/+13.5			V
Output Voltage Swing	V_O	V_S = ±15 V, R_L = 10 kΩ	±13	±14		±13	±14		±13	±14		V
		R_L = 2 kΩ	±10	±11		±10	±11		±10	±11		V
	V_{OH}	V+ = 5 V, V– = 0 V, R_L = 2 kΩ	3.9	4.1		3.9	4.1		3.9	4.1		V
	V_{OL}	V+ = 5 V, V– = 0 V, R_L = 10 kΩ		100	500		100	500		100	500	µV
Common-Mode Rejection Ratio	CMRR	V+ = 5 V, V– = 0 V, 0 V < V_{CM} < 3.5 V	90	110		80	100		800	100		dB
		V_S = ±15 V, –15 V < V_{CM} < +13.5 V	100	120		90	110		90	110		dB
Power Supply Rejection Ratio	PSRR			1.0	5.6		3.2	10		5.6	17.8	µV/V
Supply Current (All Amplifiers)	I_{SY}	V_S = ±1.5 V, No Load		65	100		65	100		60	100	µA
		V_S = ±15 V, No Load		80	120		80	120		75	120	µA

NOTE
*Guaranteed by CMRR test.
Specifications subject to change without notice

WAFER TEST LIMITS (@ V_S = ±1.5 V to ±15 V, T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Limits	Unit
Input Offset Voltage	V_{OS}		0.75	mV max
Input Offset Current	I_{OS}	V_{CM} = 0 V	5	nA max
Input Bias Current	I_B	V_{CM} = 0 V	20	nA max
Large Signal Voltage Gain	A_{VO}	V_S = ±15 V, V_O = ±10 V,		
		R_L = 100 kΩ	500	V/mV min
		R_L = 10 kΩ	250	V/mV min
		V+ = 5 V, V– = 0 V	125	V/mV min
		1 V < V_O < 4 V, R_L = 100 kΩ		
Input Voltage Range	IVR	V+ = 5 V, V– = 0 V	0/4	V min
		V_S = ±15 V*	–15/+13.5	V min
Output Voltage Swing	V_O	V_S = ±15 V		
		R_L = 10 kΩ	±13.5	V min
		R_L = 2 kΩ	±10.5	V min
	V_{OH}	V+ = 5 V, V– = 0 V, R_L = 2 kΩ	4.0	V min
	V_{OL}	V+ = 5 V, V– = 0 V, R_L = 10 kΩ	500	µV max
Common-Mode Rejection Ratio	CMRR	V+ = 5 V, V– = 0 V, 0 V < V_{CM} < 4 V	80	dB min
		V_S = ±15 V, –15 V < V_{CM} < +13.5 V	90	dB min
Power Supply Rejection Ratio	PSRR		10	µV/V max
Supply Current (All Amplifiers)	I_{SY}	V_S = ±15 V, No Load	80	µA max

NOTE
*Guaranteed by CMRR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

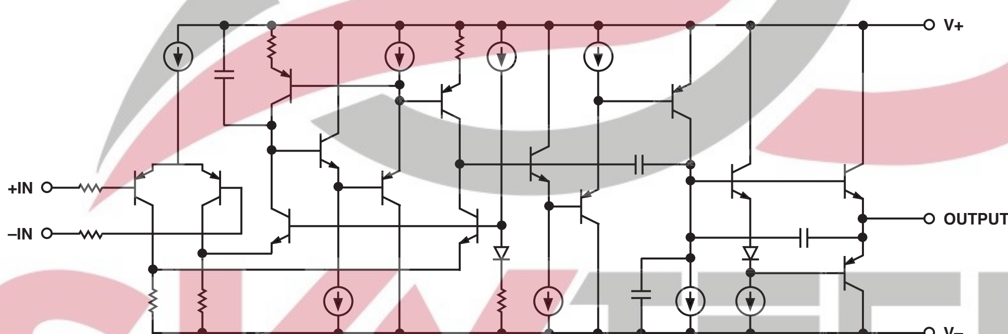


Figure 1. Simplified Schematic

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . ±18 V
Digital Input Voltage . . . . [(V–) – 20 V] to [(V+) + 20 V]
Common-Mode Input Voltage [(V–) – 20 V] to [(V+) + 20 V]
Output Short Circuit Duration . . . . Continuous
Storage Temperature Range
  Y and P Packages . . . . –65°C to +150°C
Operating Temperature Range
  OP490E, OP490F . . . . –25°C to +85°C
  OP490G . . . . –40°C to +85°C
Junction Temperature (T_J) . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}*	θ_{JC}	Unit
14-Pin Hermetic DIP (Y)	99	12	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

*θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CERDIP and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP490EY*	–25°C to +85°C	14-Lead CERDIP	Y-14
OP490FY*	–25°C to +85°C	14-Lead CERDIP	Y-14
OP490GP	–40°C to +85°C	14-Lead Plastic DIP	P-14
OP490GS	–40°C to +85°C	16-Lead SOIC	S-14

*Not recommended for new designs. Obsolete April 2002.

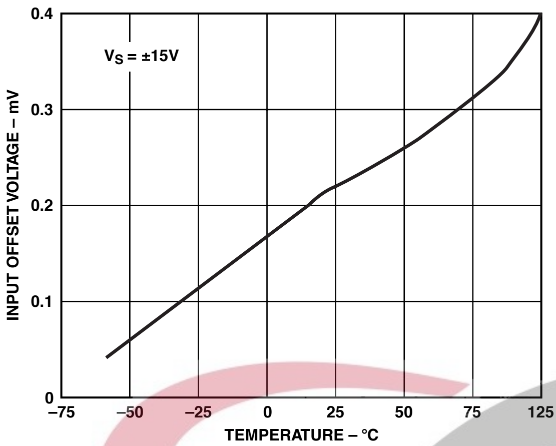
For Military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

SMD Part Number	ADI Equivalent
5962-89670013A*	OP490ATCMDA
5962-8967001CA*	OP490AYMDA

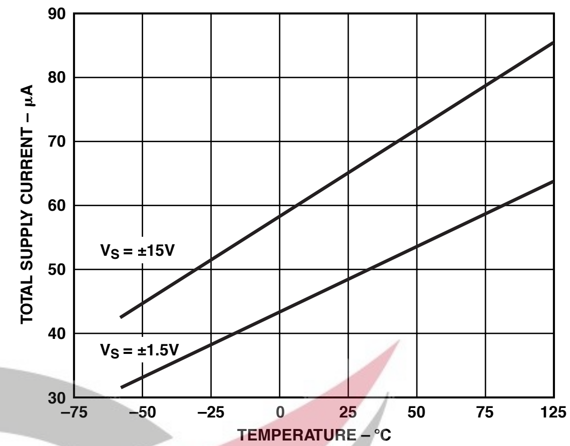
*Not recommended for new designs. Obsolete April 2002.

CAUTION

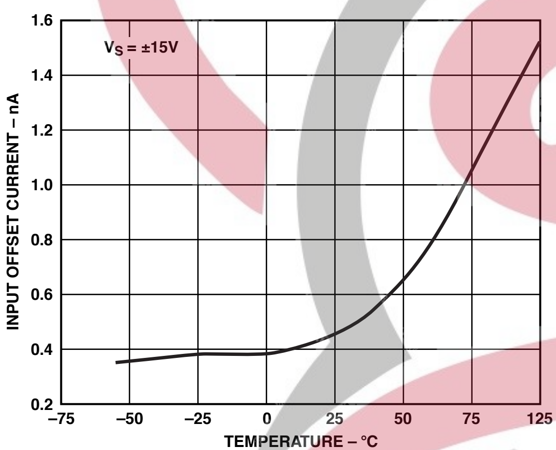
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP490 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



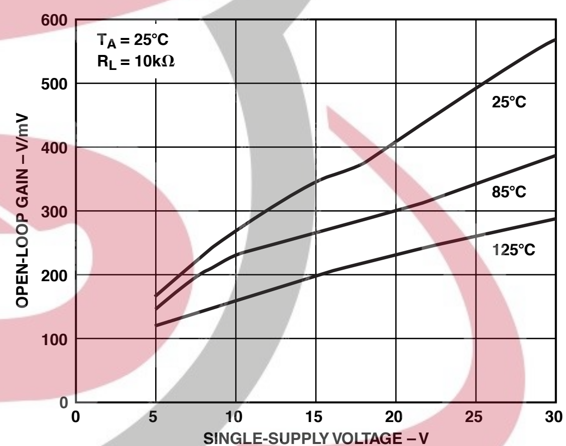
TPC 1. Input Offset Voltage vs. Temperature



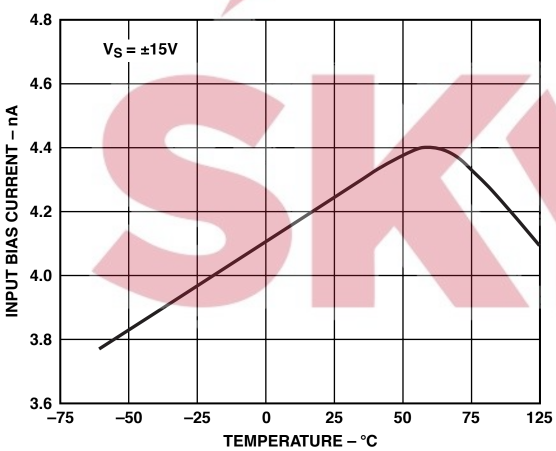
TPC 4. Total Supply Current vs. Temperature



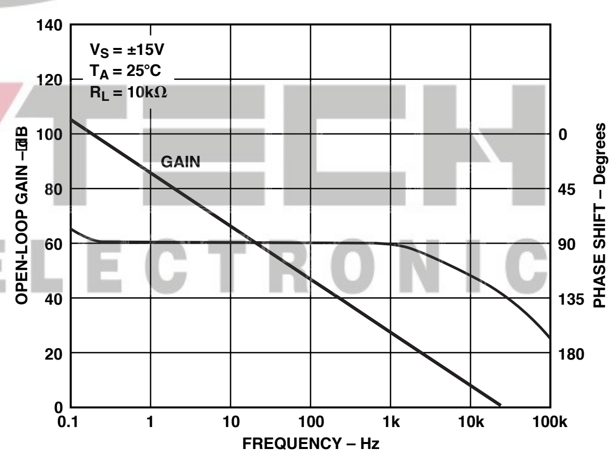
TPC 2. Input Offset Current vs. Temperature



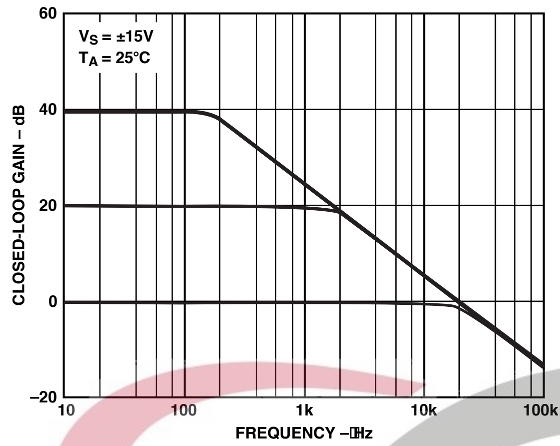
TPC 5. Open-Loop Gain vs. Single-Supply Voltage



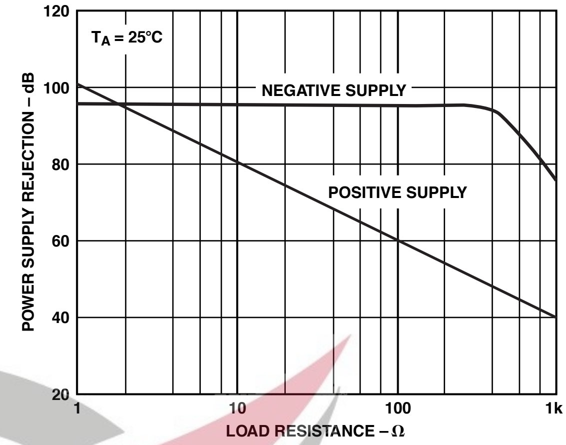
TPC 3. Input Bias Current vs. Temperature



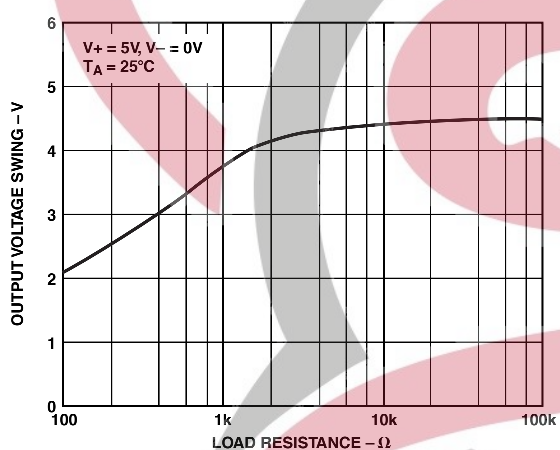
TPC 6. Open-Loop Gain and Phase Shift vs. Frequency



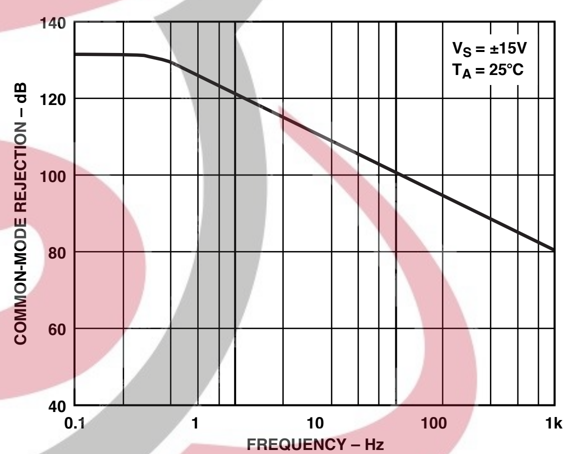
TPC 7. Closed-Loop Gain vs. Frequency



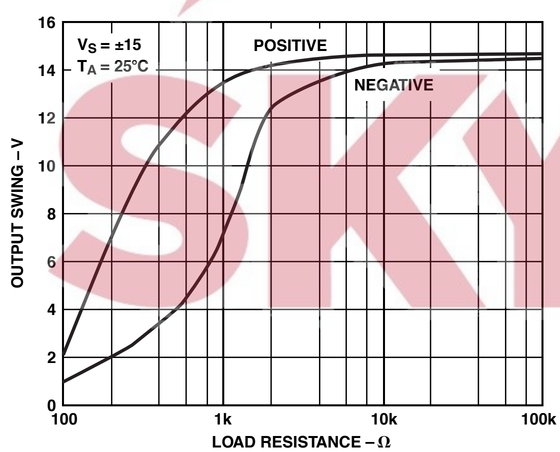
TPC 10. Power Supply Rejection vs. Frequency



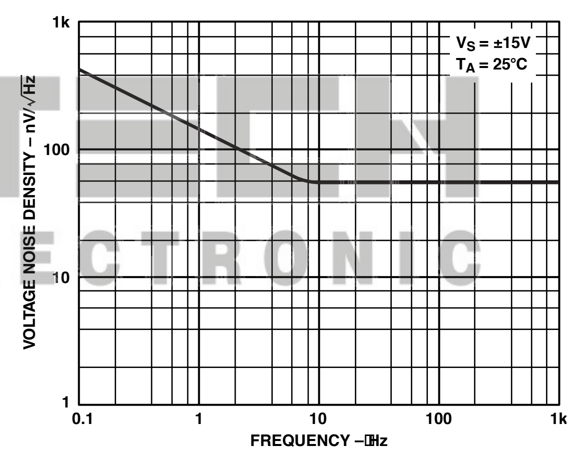
TPC 8. Output Voltage Swing vs. Load Resistance



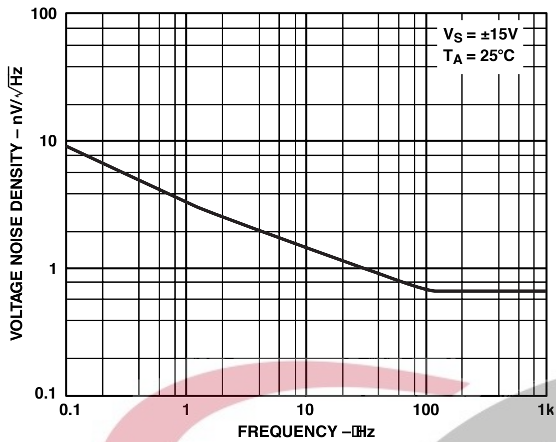
TPC 11. Common-Mode Rejection vs. Frequency



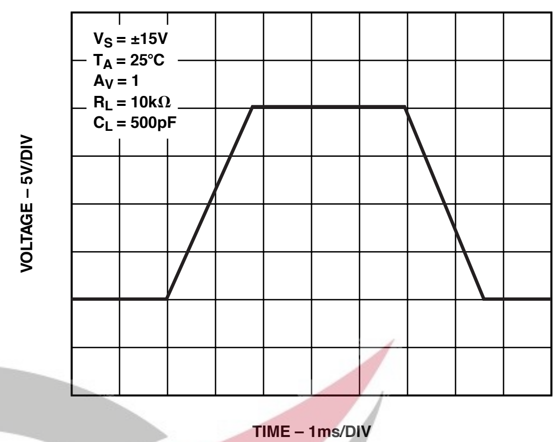
TPC 9. Output Voltage Swing vs. Load Resistance



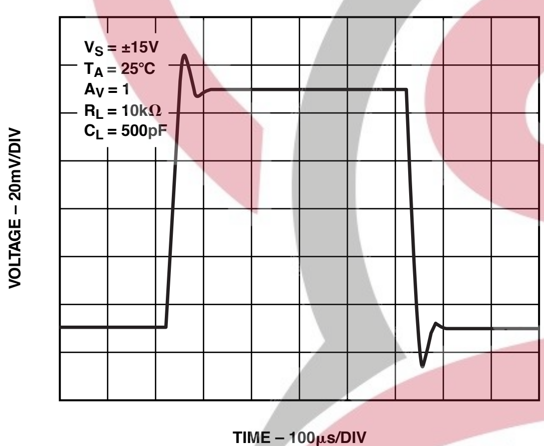
TPC 12. Noise Voltage Density vs. Frequency



TPC 13. Current Noise Density vs. Frequency



TPC 15. Large-Signal Transient Response



TPC 14. Small-Signal Transient Response

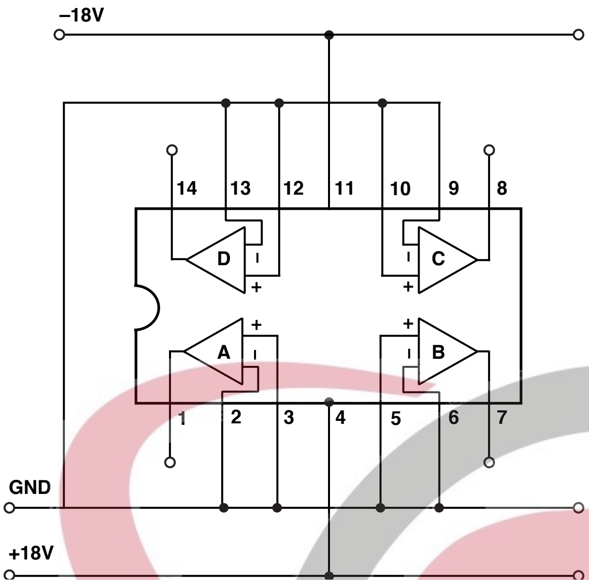


Figure 2. Burn-In Circuit

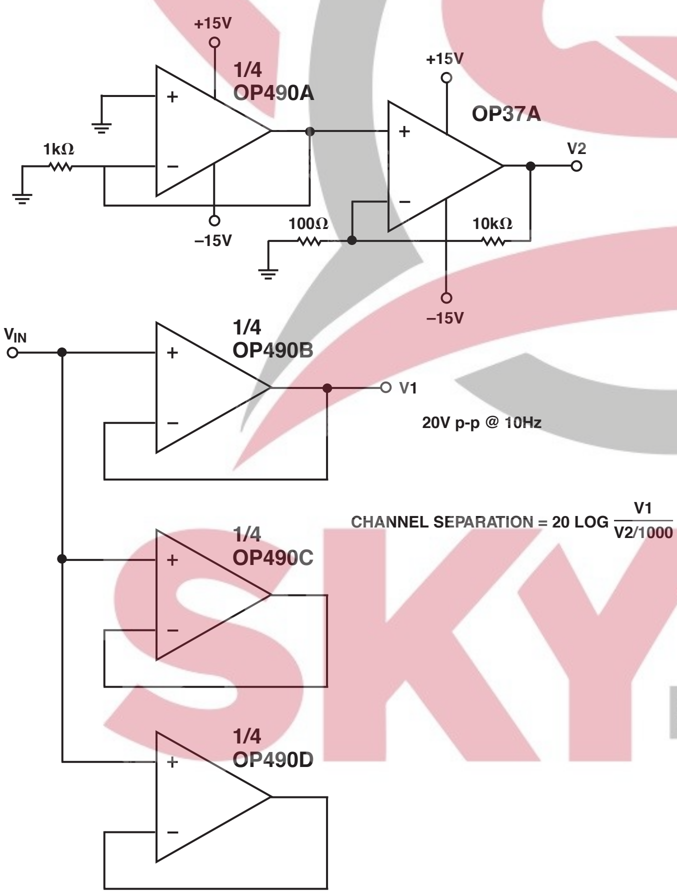


Figure 3. Channel Separation Test Circuit

APPLICATIONS INFORMATION

Battery-Powered Applications

The OP490 can be operated on a minimum supply voltage of 1.6 V, or with dual supplies of ±0.8 V, and draws only 60 μA of supply current. In many battery-powered circuits, the OP490 can be continuously operated for hundreds of hours before requiring battery replacement, reducing equipment downtime, and operating costs.

High performance portable equipment and instruments frequently use lithium cells because of their long shelf-life, light weight, and high energy density relative to older primary cells. Most lithium cells have a nominal output voltage of 3 V and are noted for a flat discharge characteristic. The low supply current

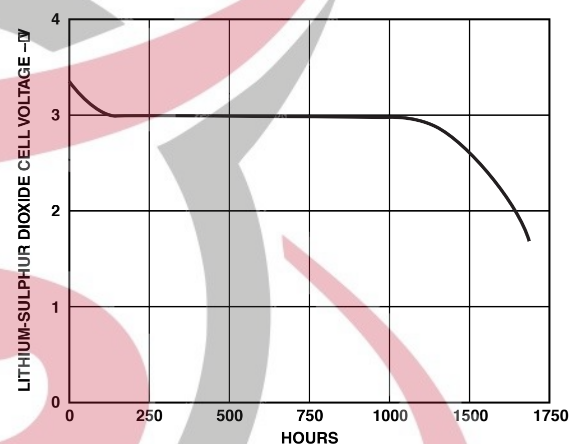


Figure 4. Lithium-Sulphur Dioxide Cell Discharge Characteristic with OP490 and 100 kΩ Loads

requirement of the OP490, combined with the flat discharge characteristic of the lithium cell, indicates that the OP490 can be operated over the entire useful life of the cell. Figure 4 shows the typical discharge characteristic of a 1 Ah lithium cell powering an OP490 with each amplifier, in turn, driving full output swing into a 100 kΩ load.

Single-Supply Output Voltage Range

In single-supply operation the OP490's input and output ranges include ground. This allows true "zero-in, zero-out" operation. The output stage provides an active pull-down to around 0.8 V above ground. Below this level, a load resistance of up to 1 MΩ to ground is required to pull the output down to zero.

In the region from ground to 0.8 V, the OP490 has voltage gain equal to the data sheet specification. Output current source capability is maintained over the entire voltage range including ground.

Input Voltage Protection

The OP490 uses a PNP input stage with protection resistors in series with the inverting and noninverting inputs. The high breakdown of the PNP transistors coupled with the protection resistors provides a large amount of input protection, allowing the inputs to be taken 20 V beyond either supply without damaging the amplifier.

Micropower Voltage-Controlled Oscillator

An OP490 in combination with an inexpensive quad CMOS switch comprise the precision V_{CO} of Figure 5. This circuit provides triangle and square wave outputs and draws only 75 µA from a 5 V supply. A acts as an integrator; S1 switches the charging current symmetrically to yield positive and negative ramps. The integrator is bounded by B which acts as a Schmitt trigger with a precise hysteresis of 1.67 V, set by resistors R5, R6, and R7, and associated CMOS switches. The resulting output of A is a triangle wave with upper and lower levels of 3.33 V and 1.67 V. The output of B is a square wave with almost rail-to-rail swing. With the components shown, frequency of operation is given by the equation:

$$f_{OUT} = V_{CONTROL}(Volts) \times 10\ Hz/V$$

but this is easily changed by varying C1. The circuit operates well up to a few hundred hertz.

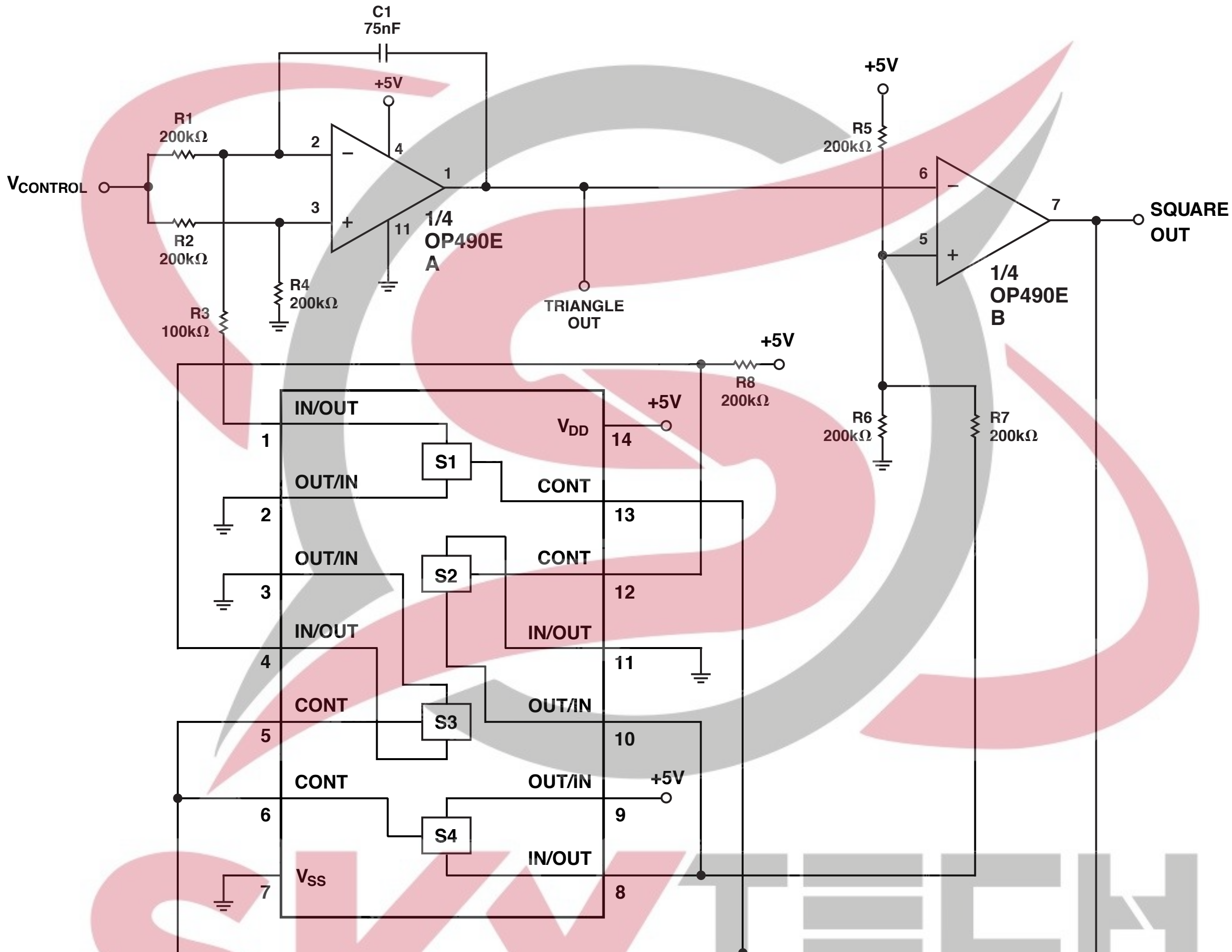


Figure 5. Micropower Voltage Controlled Oscillator

Micropower Single-Supply Quad Voltage-Output 8-Bit DAC

The circuit of Figure 6 uses the DAC8408 CMOS quad 8-bit DAC, and the OP490 to form a single-supply quad voltage-output DAC with a supply drain of only 140 µA. The DAC8408 is used in voltage switching mode and each DAC has an output resistance (≈10 kΩ) independent of the digital input code. The output amplifiers act as buffers to avoid loading the DACs. The 100 kΩ resistors ensure that the OP490 outputs will swing below 0.8 V when required.

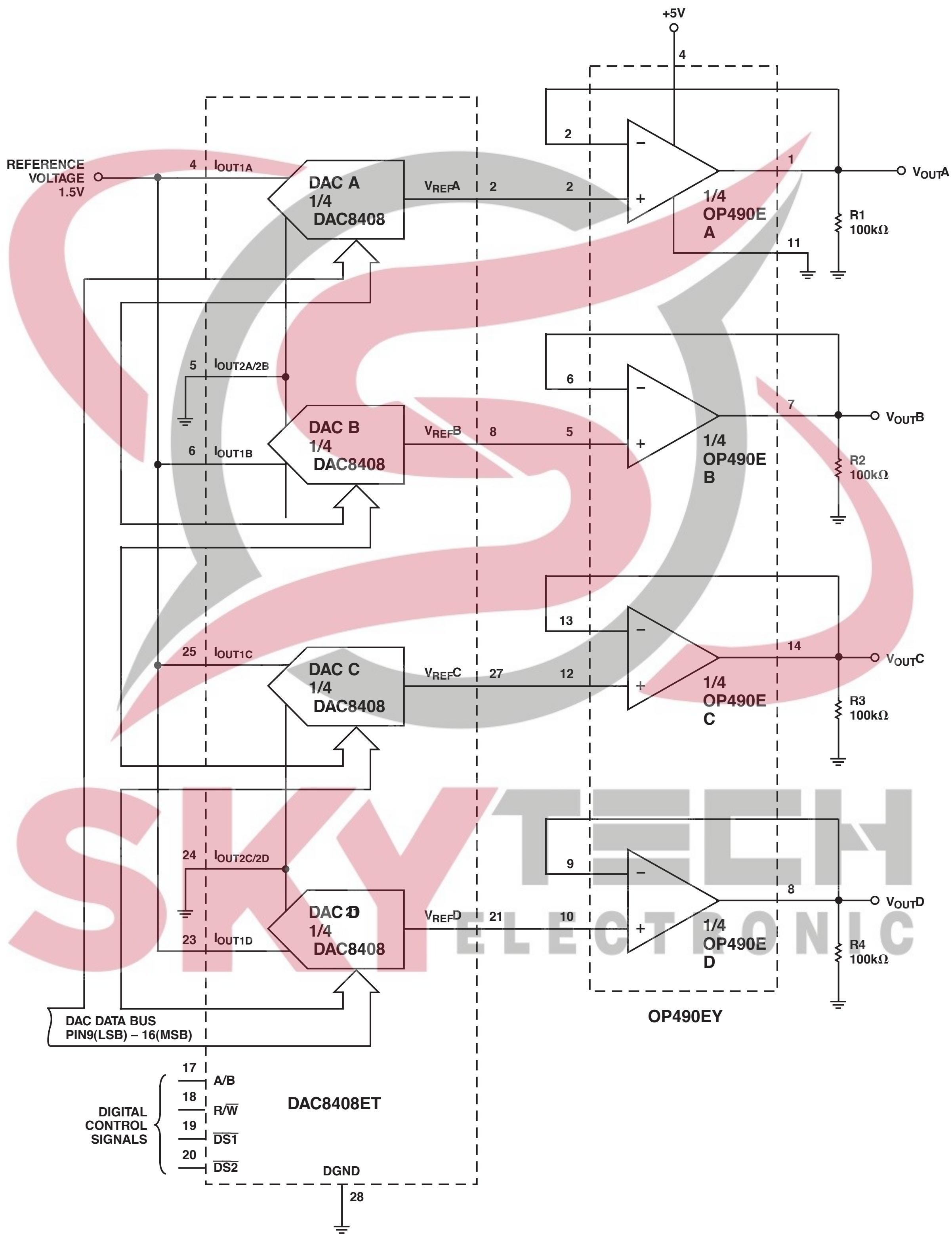


Figure 6. Micropower Single-Supply Quad Voltage Output 8-Bit DAC

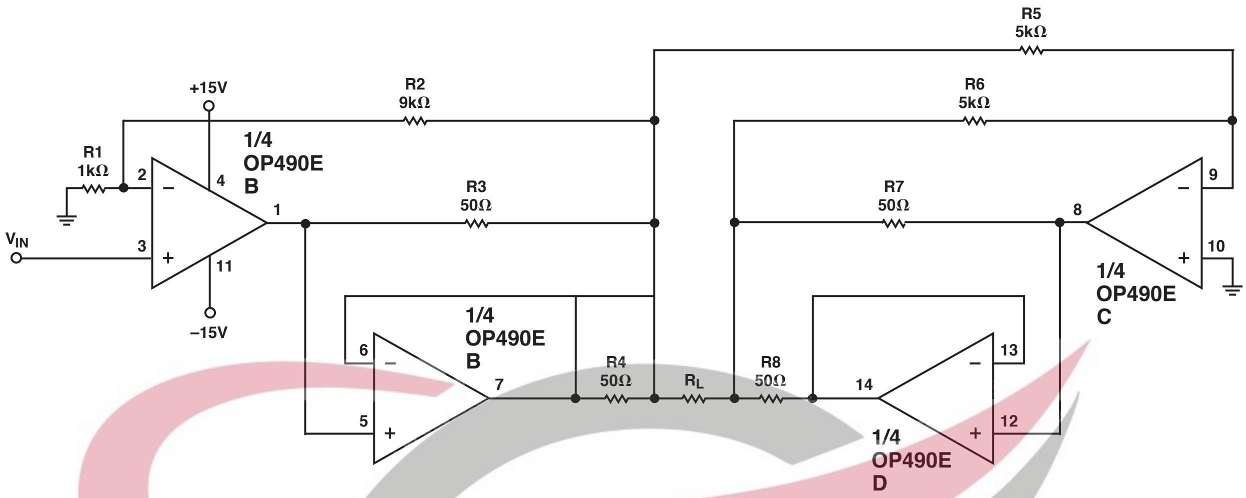


Figure 7. High Output Amplifier

High Output Amplifier
The amplifier shown in Figure 7 is capable of driving 25 V p-p into a 1 kΩ load. Design of the amplifier is based on a bridge configuration. A amplifies the input signal and drives the load with the help of B. Amplifier C is a unity-gain inverter which drives the load with help from D. Gain of the high output amplifier with the component values shown is 10, but can easily be changed by varying R1 or R2.

Single-Supply Micropower Quad Programmable Gain Amplifier
The combination of quad OP490 and the DAC8408 quad 8-bit CMOS DAC, creates a quad programmable-gain amplifier with a quiescent supply drain of only 140 µA. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the fixed DAC feedback resistor and the resistance of the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{256}{n}$$

where *n* equals the decimal equivalent of the 8-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop will be open causing the op amp output to saturate. The 10 MΩ resistors placed in parallel with the DAC feedback loop eliminates this problem with a very small reduction in gain accuracy. The 2.5 V reference biases the amplifiers to the center of the linear region providing maximum output swing.

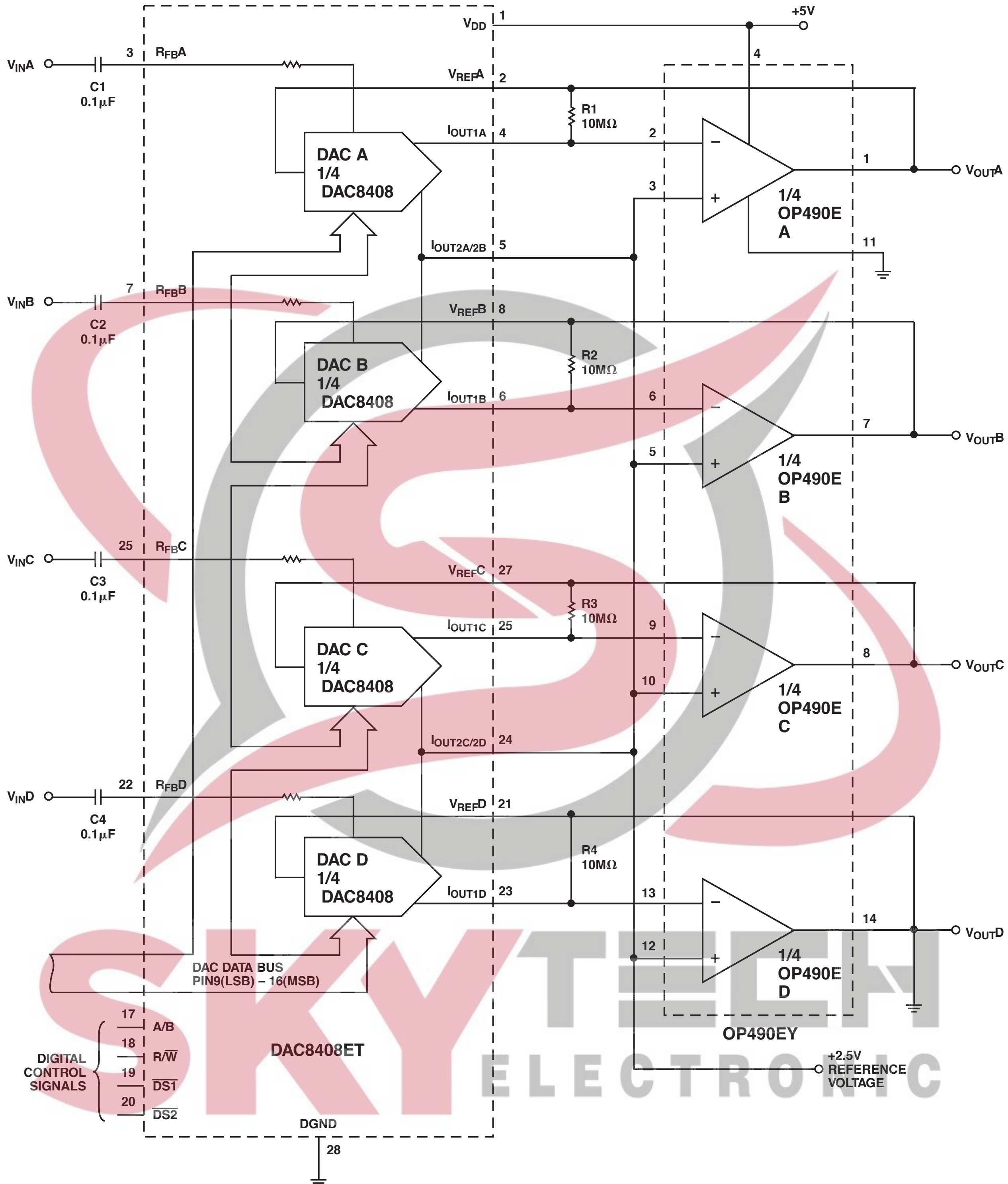
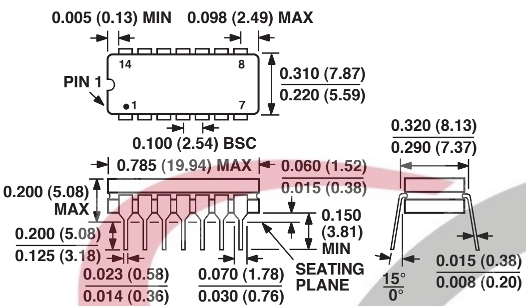


Figure 8. Single-Supply Micropower Quad Programmable Gain Amplifier

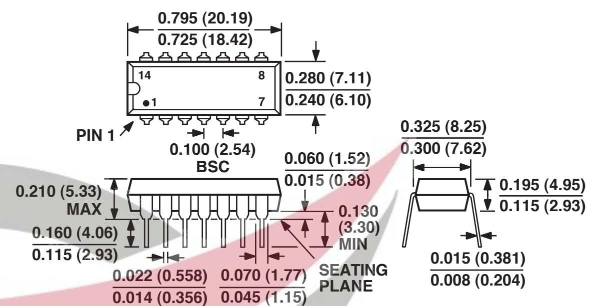
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

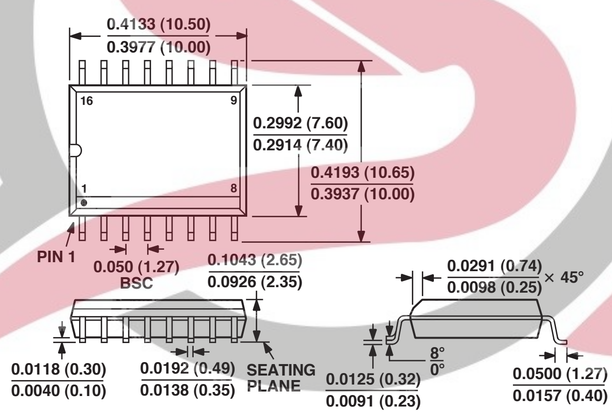
14-Lead Hermetic DIP (Y Suffix)



14-Lead Plastic DIP (P Suffix)



16-Lead SOIC (S Suffix)



Revision History

Location	Page
Data Sheet changed from REV. B to REV. C.	
Deleted 28-Pin LCC (TC-Suffix) PIN CONNECTION DIAGRAM	1
Deleted ELECTRICAL CHARACTERISTICS	3
Edits to ABSOLUTE MAXIMUM RATINGS	5
Edits to ORDERING GUIDE	5

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